What is claimed is:

1. Circuitry for reducing power dissipation in a integrated circuit, comprising:

a data latch for storing a first multibit digital signal;

an input data latch for receiving a second multibit digital signal, said input data latch producing transformed and untransformed versions of said second multibit digital signal;

a comparing circuit for comparing values of bits in respective bit positions of said first and second multibit digital signals and producing an output signal representative of a state transition at each bit position;

summing circuitry coupled to said comparing circuitry for providing a sum of state transitions for each comparison of said multibit digital signals;

a controller for determining if said sum exceeds a predetermined value, and producing a transformation vector signal in response thereto;

a selection circuit coupled to said input data latch for selecting one of said transformed and said untransformed versions of said second multibit digital signal in response to said transformation vector signal.

2. The circuitry of claim 1 wherein said comparing circuit is an exclusive-OR gate.

3. The circuitry of claim 2 wherein said controller performs a digital value comparison based on the values of the sum and a value representative of predetermined value.

4. The circuitry of claim 3 wherein said predetermined value is one-half the number of bits of said multibit data signal.

5. The circuitry of claim 4 wherein said transformed version of said second multibit digital signal is generated by inverting all bits of said second multibit digital signal in response to said transformation vector signal.

6. The circuitry of claim 5 wherein said selection circuitry is a first 2-to-1 multiplexor for selecting between said transformed and said untransformed versions of said second multibit digital signal.

7. The circuitry of claim 6 further including:

circuitry for conveying said transformation vector signal in parallel with said multibit digital signal; and

reverse transformation circuitry for restoring said transformed version of said second multibit digital signal to its original form in response in response to said transformation vector signal.

8. The circuitry of claim 7 wherein said reverse transformation circuitry is a second 2-to-1 multiplexor for selecting between inverted and non-inverted versions of said second multibit digital signal in response to said transformation vector signal.

9. A method for reducing power dissipation in a integrated circuit, comprising the steps of:

storing a first multibit digital signal;

receiving a second multibit digital signal;

producing transformed and untransformed versions of said second multibit digital signal;

comparing values of bits in respective bit positions of said first and second multibit digital signals and producing an output signal representative of a state transition at each bit position;

providing a sum of state transitions for each comparison of said multibit digital signals;

determining if said sum exceeds a predetermined value, and producing a transformation vector signal in response thereto;

selecting one of said transformed and said untransformed versions of said second multibit digital signal in response to said transformation vector signal.

10. The method of claim 9 wherein said comparing step employs an exclusive-OR function.

11. The method of claim 10 wherein said determining step is a digital value comparison based on the values of the sum and a value representative of predetermined value.

12. The method of claim 11 wherein said predetermined value is one-half the number of bits of said multibit data signal.

13. The method of claim 12 wherein said transformed version of said second multibit digital signal is generated by inverting all bits of said second multibit digital signal in response to said transformation vector signal.

14. The method of claim 13 wherein said selection step employs a first 2-to-1 multiplexor for selecting between said transformed and said untransformed versions of said second multibit digital signal.

15. The method of claim 14 further including the steps of:

conveying said transformation vector signal in parallel with said multibit digital signal; and

restoring said transformed version of said second multibit digital signal to its original form in response in response to said transformation vector signal.

16. The method of claim 15 wherein said reverse transformation employs a second 2-to-1 multiplexor for selecting between inverted and non-inverted versions of said second multibit digital signal in response to said transformation vector signal.